THE CLAIMS

What is claimed is:

1. A preventive treatment method for a multilayer semiconductor wafer that includes a supporting substrate, at least one intermediate layer and a surface layer in which an intermediate layer has an exposed lateral edge and the wafer is to be subjected to a subsequent treatment, which method comprises encapsulating the exposed lateral edge of the intermediate layer with a portion of the surface layer to prevent attack on the peripheral edge during the subsequent treatment.

2. The method of claim 1 wherein the encapsulating comprises annealing the wafer by heated to a temperature and for a time sufficient to cause the surface layer portion to cover the exposed lateral edge of the intermediate layer.

3. The method of claim 2 wherein the annealing comprises a rapid thermal annealing conducted at a temperature about 1150°C to 1300°C for a time of about 1 to 5 minutes.

4. The method of claim 3 wherein the annealing temperature is on the order of about 1200°C and the annealing time is less than about 3 minutes.

5. The method of claim 3 wherein the annealing is conducted under an atmosphere of hydrogen or argon.

6. The method of claim 1 wherein the multilayer semiconductor wafer has a silicon on insulator structure.

7. The method of claim 1 wherein the multilayer semiconductor wafer is formed by transferring at least the surface layer from a donor wafer to at least one intermediate layer by a layer transfer technique.

8. The method of claim 7 wherein the surface layer is transferred by forming a zone of weakness in the donor wafer at a depth sufficient to define the surface layer, bonding the surface layer of the donor wafer to the intermediate layer of the supporting substrate and then detaching the surface layer from the donor wafer.

9. The method of claim 8 wherein the zone of weakness is formed by implanting ions into the donor wafer.

10. The method of claim 1 which further comprises subjecting the wafer to the subsequent treatment without detrimentally affecting the edge of the intermediate layer.

11. The method of claim 10 wherein the subsequent treatment is a chemical attack or a prolonged high temperature heat treatment.

12. The method of claim 1 which further comprises subjecting the wafer to a stabox process prior to encapsulating the exposed edge of the intermediate layer.

13. A multilayer semiconductor wafer that includes a supporting substrate, at least one intermediate layer having an exposed lateral edge, and a surface layer, wherein the exposed lateral edge of the intermediate layer is encapsulated with a portion of the surface layer to prevent attack on the peripheral edge during subsequent treatments.

14. The wafer of claim 13 in the form of a silicon on insulator structure.